UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/109,261	06/30/1998	GANG BAI	042390.P5769	3347

7590 07/28/2004

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
SEVENTH FLOOR
12400 WILSHIRE BOULEVARD
LOS ANGELES, CA 90025

EXAMINER	
WARREN, MATTHEW E	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 07/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/109,261	BAI, GANG	
	Examiner	Art Unit	
	Matthew E Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-10,13-17,20 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-10,13-17,20 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the RCE and Amendment filed on July 9, 2004.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8-10, 13-17, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagata et al. (US 4,015,281) in view of Momose et al. (US 5,990,516) and Moon (US 5,621,681).

Nagata discloses (col. 3, line 45 – col. 4, line 67) a transistor device having a gate electrode overlying a gate dielectric formed directly on a semiconductor substrate. The dielectric (col. 4, lines 34-49) comprises a first dielectric having a first dielectric constant and a second dielectric having a second dielectric constant different from the first dielectric constant. The first and second dielectrics are scalable for a set of feature size technologies, wherein the first and second dielectric thickness are determined by the formula as recited in claims 8 and 15 (see the expanded formula in col. 4, lines 39-44). The second dielectric (Al_2O_3) has a greater dielectric constant than the first dielectric (SiO_2) (col. 4, lines 45-49). A third dielectric (SiO_2-P_2O_5), having a third dielectric constant may also be used in the composite dielectric layer (col. 4, lines 50-

56). Nagata et al. shows all of the elements of the claims except the set of feature size technologies defined by a gate length in the range of 25-150 nm. Momose et al. discloses (col. 16, 28-48 and col. 16, line 66-col. 17, line 32) a semiconductor device having double layer gate dielectric in which the feature size technology has a gate length of 150 nm (or 0.15 μm) to form a high performance semiconductor having low power consumption. Momose et al. further discloses (col. 15, lines 13-31) that the gate length can be decreased even more to improve the current drive capability. The gate in one embodiment had a length of 40 nm (0.04 μm). Momose et al. also discloses (col. 2, lines 52-58) a semiconductor device in which the gate dielectric is less than 1/3 the gate length. The thin gate dielectric improves hot carrier reliability and ultimately the operating characteristics. Nagata and Momose shows all of the elements of the claims except the first dielectric selected from the group of HfO_2, BaO, La_2O_2, Y_2O_3 and ZrO_2. Moon shows a (fig. 2) a semiconductor device comprising a first dielectric material (11a) of Y_2O_3 and a second dielectric material (12a) of PZT which has a second dielectric constant greater than the dielectric constant of the first dielectric. With this configuration, the yttrium oxide is used as a buffer dielectric and a good quality ferroelectric is formed on the substrate. Moon also shows that the transistor device is isolated from other devices by shallow trench isolation (2). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the multi-layer gate dielectric of Nagata for a feature size technology with a desired gate length as taught by Momose to form a high performance transistor having low power consumption. It would have been obvious to one of ordinary skill in the art at the time the invention was made

to modify the multiplayer gate dielectric of Nagata and Momose by using Y_2O_3 and PZT as the first and second dielectric layer as taught by Moon to form a good quality ferroelectric on a substrate.

Response to Arguments

Applicant's arguments filed with respect to claims 8-10, 13-17, 20 and 21 have been fully considered but they are not persuasive. The applicant primarily asserts that the cited references do not show the added limitation of the transistor devices being isolated from other devices by shallow trench structures. The examiner believes that the cited references show all of the elements of the claims including the added limitation of the shallow trench structure. As stated in the rejection above, Moon shows in figure 2 shallow trench isolation structures (2) to separate components on a semiconductor substrate. Moon even states in column 4, lines 59-67 that isolation structure (2) is formed by a STI (shallow trench method). Furthermore, it is notoriously well known in the art that semiconductor devices are separated from each other by isolation oxides, structures, etc. An array of MOSFETs, MISFETS, IGFETS, etc. will be isolated from peripheral devices, such as capacitors, ROMs, DRAMs, ESD circuits, etc. by isolation oxides. Therefore, the cited references show all of the elements of the claims and the rejection remains proper.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MEW
MEW
July 26, 2004

Tom Thomas
TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800